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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HUFFMAN LAW GROUP, P.C.
1832 N. CASCADE AVE.
COLORADO SPRINGS, CO 80907-7449

EXAMINER	
COLEMAN, ERIC	
ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,084	UHLER, G. MICHAEL	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-20,22-28 and 30-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17-20,22-28,30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

The Examiner regrets that the art cited and rejections in the action were not presented earlier.

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 28-33 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

3. Claim 28 is directed to a computer program product comprising a computer usable medium, having program code embodied in the medium. The medium is not limited to a implementation that is tangibly embodied so as to be executable by the computer (such as computer readable storage medium). The claimed computer usable medium is within the scope of transmission mediums that are not tangible. Therefore claim 28 and the claims that depend from claim 28 (claims 29-30) are also non-statutory.

4. Claim 31, is directed to a data signal embodied in a transmission medium. A transmission medium is not tangible in any manner that can be executed by an computer. Therefore the claimed invention is non-statutory. [Note a functional data stored computer readable storage medium does provide for interrelationship with computer such that the functional data become tangibly embodied so as to be executable]. Therefore the claims the claims that depend from claim 31 (claims 32,33) are also non-statutory].

Claim Rejections - 35 USC § 102

5. Claims 1,2,3,10,23,28,31 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen (patent No. 5,115,506).

6. Cohen taught the invention as claimed including a data processing ("DP") system comprising (As per claim 1):

7. A plurality of register sets (Normal register set and alternate register set)(e.g, see figs 1a, 1b); an interrupt vector generator for generating an exception vector associating with the interrupt handler, when the processing system receives and interrupt (e.g., see fig. 2 and col. 3, line 64-col. 4, line 8); mapping logic coupled to both of the register sets and the interrupt vector generator for selecting on of said plurality of register sets to be used by the interrupt handler (e.g., see col. 3, lines 13-45) wherein the mapping logic is programmably provided with a correlation between the exception vector and the selected on of the plurality of register sets (e.g., see col. 3, lines 13-45). As to the limitation of the register sets being shadow register sets the only requirement of the registers sets to be shadow register sets is that they are the same in size. Each of the registers sets of Cohen are the same as the other register set and therefore each provides a separate shadow register set. Together they provide for plural shadow register sets. Also the programmability is not provided for by the elements in the claim and therefore the programmable providing of the mapping logic is given no weight.

8. As the limitations of claim 28, 31, where the features discussed above are claimed as program code for providing the elements claimed since Cohen system comprised processor on a semiconductor chip that provided for interrupts it would have

been anticipated that the features would have been programmed for controlling the elements as discussed above. The use of hardware or software for the particular portions operation are equivalent implementations merely determined depending on cost/speed necessary for the system.

9. As per claim 2, Cohen taught each of the plurality of shadow register sets compromise a plurality of duplicate register sets comprise a plurality of registers that duplicate registers of a general purpose (GPR set) (e.g., see col. 3, lines 7-28).

10. As per claim 3, Cohen taught the correlation comprises a maps an exception vector to one of said plurality of shadow register sets (e.g., see col. 3, lines 29-63).

11. As per claim 10, Cohen taught a status register, for storing data corresponding to a current shadow set, and a previous shadow set (e.g., see CSC register and CSC' register (e.g., see fig. 1C).

12. As per claim 23, Cohen taught a microprocessor (semiconductor chip 12 with CPU 14) having a first register set (normal register set) for use by non-interrupt instructions, and a second (Normal register set) and third register sets(alternate register) for use by interrupt service routines the microprocessor comprising: a vector generator, for generating exception vectors corresponding to the interrupt service routines; and mapping logic, coupled to said vector generator, for selecting between the second and third register sets for use by the interrupt service routines based on a value of said exception vectors interrupt (e.g., see fig. 2 and col. 3, line 64-col. 4, line 8)[Cohen taught in the body of the claim and plurality shadow registers however does not

reference first register set and does not require the first register set and therefore the use of a first register set is given no weight.

13. Claims 1,2,3,4,7,8,9,14,15,20,22,23,26,27,28,31 are rejected under 35 U.S.C. 102(b) as being anticipated by Maupin (patent No. 6,154,832) Maupin taught invention as claimed comprising a data processing ("DP") system comprising: (As per claims 1,2,14,20,22,23): a plurality of shadow register sets with addressable registers (46a,46b,46c,46d, 46e,46f,46g) a least one for default task and plurality of register sets each shadow register set dedicated to a different interrupt source (e.g., see col. 2, lines 56-64); interrupt vector generator (e.g., see col. 5, lines 35-44) and shadow set mapping logic coupled to register sets and interrupt generator (e.g., see col. 6, lines 16-32)[task-Ids assigned to interrupt sources and execution core correlates task-ID to interrupt source and using interrupt task-ID to select register set (46a-46H).

14. As the limitations of claim 28, 31, where the features discussed above are claimed as program code for providing the elements claimed since Maupin system comprised processor on a semiconductor chip that provided for interrupts it would have been anticipated that the features would have been programmed for controlling the elements as discussed above. The use of hardware or software for the particular portions operation are equivalent implementations merely determined depending on cost/speed necessary for the system.

15. As per claim 3, Maupin taught the correlation comprises a map register that maps the exception vector to a selected one of the plurality of register sets (task-id register) e.g., see col.5, lines 35-55 and col. 6, lines 16-28)[value in the task register used to map the exception vector or interrupt source to register set];

16. As per claim 4 Maupin taught the interrupt vector generator selects a particular one of a plurality of interrupt routines to be used to handle the interrupt (e.g., see col. 5, lines 34-44);

17. As per claim 7, 14 Maupin taught a mapping logic comprising a plurality of programmable fields, each corresponding to one of a plurality of exception vectors, each of the plurality of fields containing data referencing one of the plurality of shadow register sets (e.g., see col. 5, lines 34-55).

18. As to the off core and on core interrupts (claim 15), Maupin taught external source register set (46G) for external interrupts and A/D register set for internal A/D interrupt (e.g., see fig. 2 and col. 3, lines 37-67).

19. As per claim 8, Maupin taught eight different register sets and therefore since it would require four bits to select between eight register sets (e.g., see fig. 2)(one for each interrupt source) then one of ordinary skill would have been motivated to employ four bits for the programmable fields.

20. As per claim 9, 20, 22 , Maupin taught the data in each of the plurality of fields corresponds to one of plurality of shadow register sets (e.g., see col. 5, line 34-col. 6, line 2).

21. As per claim 26, 27, Maupin taught upon receipt of an interrupt, determining which one of a plurality of exception routines should be executed (e.g., see col. 4, lines 1-10); and based on the received interrupt, selecting one of a plurality of shadow register sets to be utilized by the one of the plurality of exception routines wherein the step of selecting utilizes programmable registers that contain data indicating which one of the plurality of shadow register sets is to be used for its register (e.g., see col. 4, lines 11-36). Maupin also taught that each of the programmable registers corresponds to one of the exception routines (e.g., see col. 6, lines 16-29).

Claim Rejections - 35 USC § 103

Claims 10,11,12,13,24,25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin.

22. Maupin taught the invention substantially as claimed including a data processing ("DP") system comprising: a plurality of shadow register sets with addressable registers (46a,46b,46c,46d, 46e,46f,46g) a least one for default task and plurality of register sets each shadow register set dedicated to a different interrupt source (e.g., see col. 2, lines 56-64); interrupt vector generator (e.g., see col. 5, lines 35-44) and shadow set mapping logic coupled to register sets and interrupt generator (e.g., see col. 6, lines 16-32)[task-Ids assigned to interrupt sources and execution core correlates task-ID to interrupt source and using interrupt task-ID to select register set (46a-46H).

23. As per claim 24,25 Maupin taught a status register)(storing task-Id) (e.g., see col. 6, lines 16-28) Maupin did not specifically detail the data corresponding to a current shadow set and a previous shadow set (or corresponding to first and second exception vector or data referencing either the second register set or the third register set). However the data in the register does not alter the operation of the system as claimed. This data is descriptive data and the steps performed by the system do not depend on the content of the data. The data is merely bits stored in a memory and the only difference between claimed invention and the Maupin references are only the view of the data. Nonfunctional descriptive material cannot render nonobvious an invention that would have been obvious In re Gulack, 703 F. 2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F 3d. 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

24. As per claim 10,11, Maupin taught a status register)(storing task-Id) (e.g., see col. 6, lines 16-28) Maupin did not specifically detail the data corresponding to a current shadow set and a previous shadow set (or corresponding to first and second exception vector or data referencing either the second register set or the third register set). However the data in the register does not alter the operation of the system as claimed. This data is descriptive data and the steps performed by the system do not depend on the content of the data. The data is merely bits stored in a memory and the only difference between claimed invention and the Mauping and and Mano references are only the view of the data. Nonfunctional descriptive material cannot render nonobvious an invention that would have been obvious In re Gulack, 703 F. 2d 1381, 1385, 217

USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F 3d. 1579, 32 USPQ2d 1031 (Fed. Cir. 1994).

25. As per claim 12,13 The saving of the status of registers upon occurrence of an interrupt and restoring the context are the interrupt was serviced was well known in the art at the time of the claimed invention.

26. Claims 5,6,17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maupin as applied to claims 1-4,14,15 above, and further in view of M. Morris Mano (book entitled Computer system Architecture) hereafter referred to as Mano.

27. As per claim 5,18 Mano taught the selected particular one of a particular of the interrupt routines is located in a memory at the corresponding exception vector (e.g., see pages 440-441 under Software routines section).

28. As per claim 6,17, Mano taught the interrupt vector generator selected a particular one of a plurality of interrupt routines to be used to handle the interrupt based on the priority level of the interrupt (e.g., see pages 437-441).

29. As per claim 19 Maupin taught the interrupt vector generator selects a particular one of a plurality of interrupt routines to be used to handle the interrupt (e.g., see col. 5, lines 34-44).

30. As the limitations of claim 28, 30, where the features discussed above are claimed as program code for providing the elements claimed since Maupin system comprised processor on a semiconductor chip that provided for interrupts it would have been anticipated that the features would have been programmed for controlling the

elements as discussed above. The use of hardware or software for the particular portions operation are equivalent implementations merely determined depending on cost/speed necessary for the system.

31. It would have been obvious one of ordinary skill in the DP art to combine the teachings of Maupin and Mano. Maupin taught system where interrupt were generated and serviced using plural register sets (e.g., see col. 5, lines 35-44) but did not specify the circuitry for controlling the access to interrupt handling routines. Mano taught the conventional means and method for implementing the handling of interrupts in a DP system. Therefore one of ordinary skill in the DP art would have been motivated incorporate the teachings of Mano at least to implement effectively Mano teachings.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Deng (patent No. 5,539,448) disclosed a priority first come first serve interrupt controller (e.g., see abstract).

Singhal etal (article in 1988 IEEE entitled Implementing a Prolog Machine with Multiple functional Units) disclosed the use of four register sets in a processor (e.g., see page 45, column 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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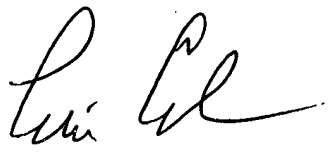

ERIC COLEMAN
PRIMARY EXAMINER